

Practical Telecom DAC Testing

By Bill Jasper



1 Introduction

Digital to analog conversion is a key component of telecom signaling, and the goal is ever higher bandwidth utilization. This paper will discuss practical issues associated with testing modern telecom DACs.

Major types of DACs include:

- Fully decoded, thermometer, string, R2R ladder, binary weighted
- Sigma Delta / Pulse width modulators
- Compounded
- Compound hybrids

Each of these DAC types has unique characteristics that are advantageous for specific applications. Modern DAC spatial ranges are up to 24 binary bits and temporal ranges are from DC to above 1GHz.

Telecommunication applications require high linearity and high bandwidth. A desirable direct conversion radio transmitter, for example, could consist of a DSP processor feeding matched quadrature DACs, followed by a quadrature up-conversion to RF. Ignoring many practical details, this single hardware platform could service a broad spectrum of modulation schemes (AM, FM, QPSK, CDMA, OFDM, etc.). Slight variations of this architecture will appear in most radio transmitter designs (see Figure 1.1).

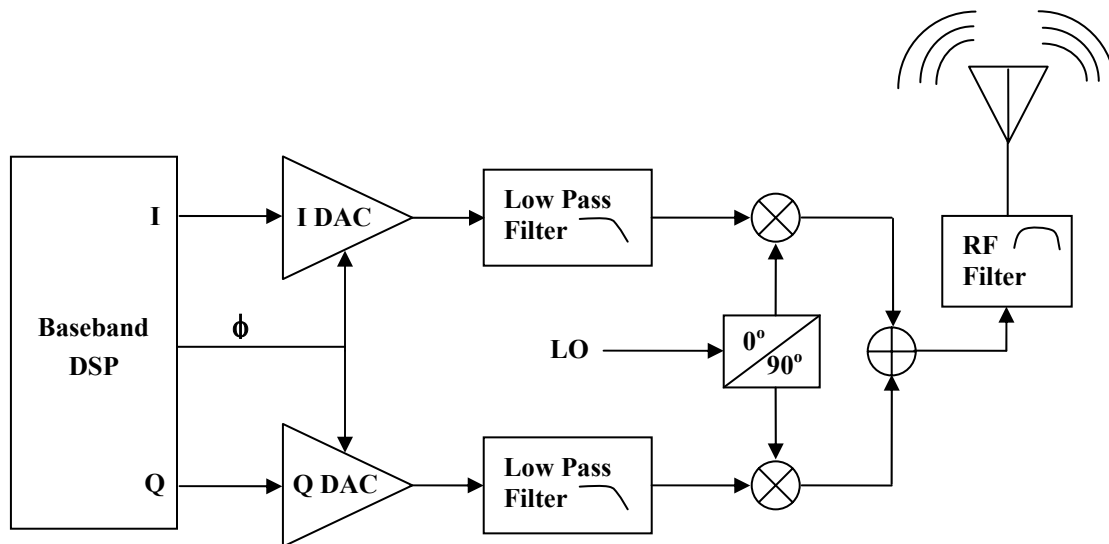


Figure 1.1

The ultimate goal is a direct signaling DAC at gigahertz rates. This single architecture could put all aspects of modulation and tuning under software control, which would be advantageous for hardware cost and complexity.

2 The Test Setup

Symbol (input) and sample (output) clocks are usually applied as a single DUT clock and input/output rates are the same. When separated, the symbol clock should be treated as digital and the sample clock as analog when considering load board design.

Capture of the analog output often requires 2 digitizers. Use a low frequency, high resolution digitizer for DC parameters and a high frequency digitizer for AC parameters. Carefully check your digitizer for sufficient resolution based on the required voltage range, DAC quantum size and parameter limits.

For low frequency measurements, check the digitizer strobe position to be sure it is clear of the analog transition time. This is best done by sweeping the strobe time across a full cycle in small increments while performing the test of interest. The transition time is easily identified by a sharp chasm or peak in the plot of the parameter of interest. Input thresholds are measured in this fashion usually using SNR as a feedback parameter.

Telecom DACs will usually need connection to a continuous spectrum analyzer. Be careful to maintain controlled transmission lines on all paths. It is often a good idea to use high bandwidth coax connectors on the load board to allow flexibility during debug and characterization. The coax connections can be hooked up to relay trees when converting to production.

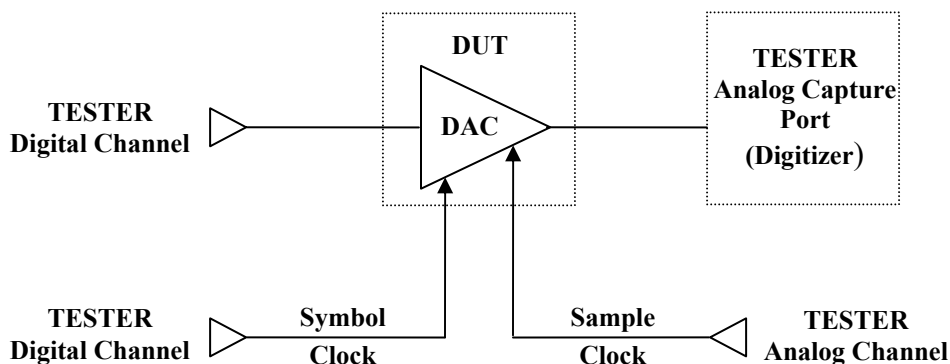


Figure 2.1

3 Measurement Units

It is very important to clearly communicate measurements. Specify AC measurements without ambiguity (e.g. V_{rms} , V_{rmsd} , V_{ptp} , dBC). Measurements are assumed single ended unless specified with d (differential) suffix. Some important relationships are:

$$V_{pk} = V_{rms} * \sqrt{2} \quad (3.1)$$

$$V_{ptp} = 2 * V_{pk} \quad (3.2)$$

$$V_{ptpd}(\text{differential}) = 2 * V_{ptp}(\text{single end}) \quad (3.3)$$

Decibels are expressed relative to a specific reference. For example dBFS is relative to full scale, dBV is relative to 1.0V, dBC is relative to the carrier, etc. For voltage ratios:

$$dBV_r = 20 * \log | V / V_r | \quad (3.4)$$

For power ratios dBm is relative to 1.0mW.

$$dBPr = 10 * \log (P / Pr) \quad (3.5)$$

And when both measured and relative power are applied to the same resistor load:

$$dBPr = 10 * \log (V^2 / Vr^2) \quad (3.6)$$

Some relationships involving common mode voltage to differentials with positive and negative nodes:

$$V_{cm} = (V_p + V_n) / 2 \quad (3.7)$$

$$V_d = V_p - V_n \quad (3.8)$$

4 DC Test Parameters

These parameters include:

- Offset Error
- Gain Error
- DNL (differential non-linearity)
- INL (integral non-linearity)
- PSS (power supply sensitivity)

4.1 Offset and Gain Error

Gain and offset are extracted from a sample set of pair values. Each pair consists of digital code in and analog voltage out. These complete set of pair points constitute the DAC transfer curve (usually a line). The slope of the line is the DAC's inherent gain and the offset is some agreed upon point offset to a zero reference. The general transfer curve of the DAC can be represented by the familiar equation:

$$y = mx + b \tag{4.1}$$

where DAC gain is m and DAC offset is b.

There are 2 main methods for determining gain and offset. First is the endpoint method which sets gain based on the minimum scale and full scale points. Offset is determined from either of the endpoints or a mid point code.

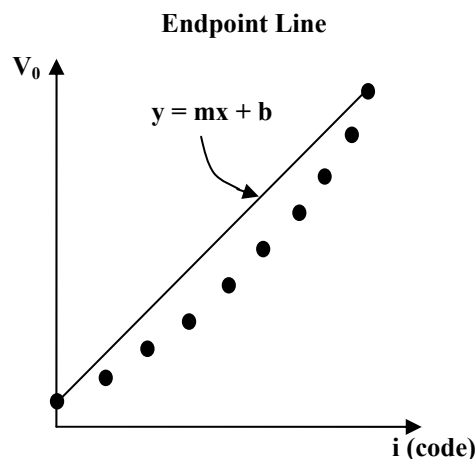


Figure 4.1

A preferred technique is the best-fit line. The m and b (gain and offset) parameters are set based on the minimum mean squared error (MMSE) distance (from line to sample).

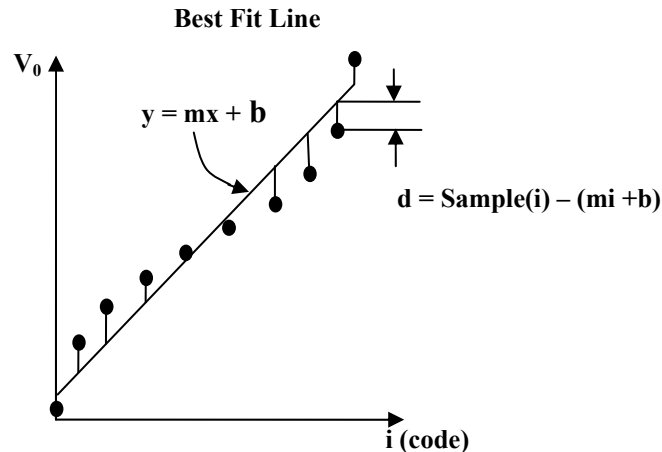


Figure 4.2

With MMSE the line is based on the total sample set without favoritism to a few points. Squaring the distance has the effect of magnifying large distances and shrinking small distances. There are various techniques for calculating the m and b parameters of the best fit line. A common method minimizes the partial derivatives with respect to slope and offset of the squared distances between the best-fit line and sample set¹. The equations derived from this method are:

$$\text{gain} = \frac{N K_4 - K_1 K_2}{N K_3 - K_1^2} \quad \text{offset} = \frac{K_2}{N} - \text{gain} \frac{K_1}{N} \quad (4.2a, 4.2b)$$

where

$$K_1 = \sum_{i=0}^{N-1} i \quad K_2 = \sum_{i=0}^{N-1} S(i) \quad K_3 = \sum_{i=0}^{N-1} i^2 \quad K_4 = \sum_{i=0}^{N-1} iS(i) \quad (4.3a-d)$$

These formulas are easily implemented inside the test program to produce the m and b parameters of the best-fit line. The m parameter is gain in units of volts per quantum step. Gain error is usually reported normalized as a percent:

$$G_{\text{err}} = \frac{(m_{\text{bestfit}} - m_{\text{target}})}{m_{\text{target}}} * 100 \quad (\%) \quad (4.4)$$

Target m is the target gain the DAC was designed to.

Offset error is usually reported with respect to the DAC zero code. The zero code could occur at V_{\min} if binary encoded or at V_{mid} if twos complement encoded. Be sure to pay attention to details of code positions. The zero code of twos complement is actually $\frac{1}{2}$ quantum above mid scale. Offset error is usually reported normalized to LSB (quantum) units where V_{lsb} is the slope (m) of the best-fit line.

$$Off_{\text{err}} = \frac{((m_{\text{bestfit}} \times i_0 + b_{\text{bestfit}}) - V_{\text{Off}_{\text{target}}})}{V_{\text{lsb}}} \quad (\text{LSB}) \quad (4.5)$$

Offset and gain match are important parameters for quadrature DAC pairs and usually required to be well below 1 LSB.

4.2 DNL and Monotonicity

Differential non-linearity is a metric of uniformity of the individual quanta step sizes. Use the previously collected DAC transfer data points. DNL consists of a set of N-1 data values. Each value is the difference between the actual step size and the LSB (quantum) step size normalized to one quantum:

$$\text{DNL}(i) = \frac{(S(i+1) - S(i) - V_{\text{lsb}})}{V_{\text{lsb}}} \quad (\text{LSB}) \quad (4.6)$$

In order to remove gain from the DNL metric V_{lsb} should be the slope of the best-fit line. Other means of calculating V_{lsb} have varying degrees of effect on DNL (although mostly negligible). The order of methods from most relaxed to most demanding is best-inl line, best-fit line, endpoint and design target. DNL can be reported as the full set of values in ascending code order to correlate with the DAC architecture. DNL can also be reported as the worst case positive and/or negative values of the set to be compared with pass/fail limits.

Monotonicity is defined as continuously increasing (or decreasing), i.e. $S(i+1) \geq S(i)$ for all samples.

4.3 INL

Integral non-linearity is a metric of cumulative match of the DAC transfer set to the best-fit line. One could also compare to the endpoint line or target design but these methods would include gain error. INL consists of a set of N data values. Each value is the difference between the sample point and the best-fit line and normalized to one quantum (v_{lsb}):

$$\text{INL}(i) = \frac{(S(i) - (m_{\text{bestfit}} \times i_0 + b_{\text{bestfit}}))}{V_{\text{lsb}}} \quad (\text{LSB}) \quad (4.7)$$

INL is the integral of the DNL curve and can also be calculated as the running sum of DNL values:

$$\text{INL}(i) = \frac{\sum_{j=0}^{i-1} \text{DNL}(j) + S(0) - (m_{\text{bestfit}} X i + b_{\text{bestfit}})}{V_{\text{lsb}}} \quad (\text{LSB}) \quad (4.8)$$

And conversely, DNL can be calculated by taking the first derivative of the INL curve:

$$\text{DNL}(i) = \text{INL}(i+1) - \text{INL}(i) \quad (\text{LSB}) \quad (4.9)$$

For DAC test it is convenient to calculate DNL from INL whereas for ADC test it might be more convenient to calculate INL from DNL. Like DNL, INL can be reported by all values in order or by worst case positive and negative values against limits.

4.4 Power Supply Sensitivity

Characterization of medium and low frequency power supply sensitivity is effectively done with the usual corners of the DC power supply voltage.

5 AC Test Parameters

There are several parameters that measure the AC performance of the DAC circuit:

- Settling or conversion time
- Slew time
- Glitch energy
- Crosstalk
- DAC-to-DAC skew
- Spectra (noise and distortion)

Note that when creating code patterns for monotone or multitone tests, it is important to follow the guidelines of DSP.

- Pick M relatively prime to N
- Pick M and F_s so that aliased harmonics don't share a common bin
- Randomize the phase of multitones to minimize the peak to RMS level ratio
- The FFT usually returns V_{pk} amplitude bins

5.1 Settling, Slew, and Glitch Energy

The DAC output looks like a staircase with unsettled transitions sometimes termed conversion time (see Figure 5.1). These parameters are best observed with high bandwidth instruments often outside the capability of ATE. High speed DACs are usually observed with a high bandwidth oscilloscope on transitions from minus full scale to plus full scale (largest voltage swings) and rarely measured in production. Rise time is usually measured at 10/90% or 20/80%. Settling time is typically described to within $\frac{1}{2}$ LSB. And glitch energy is an integral voltage-time product of the area outside of a $\frac{1}{2}$ LSB error band in units of ps-V.

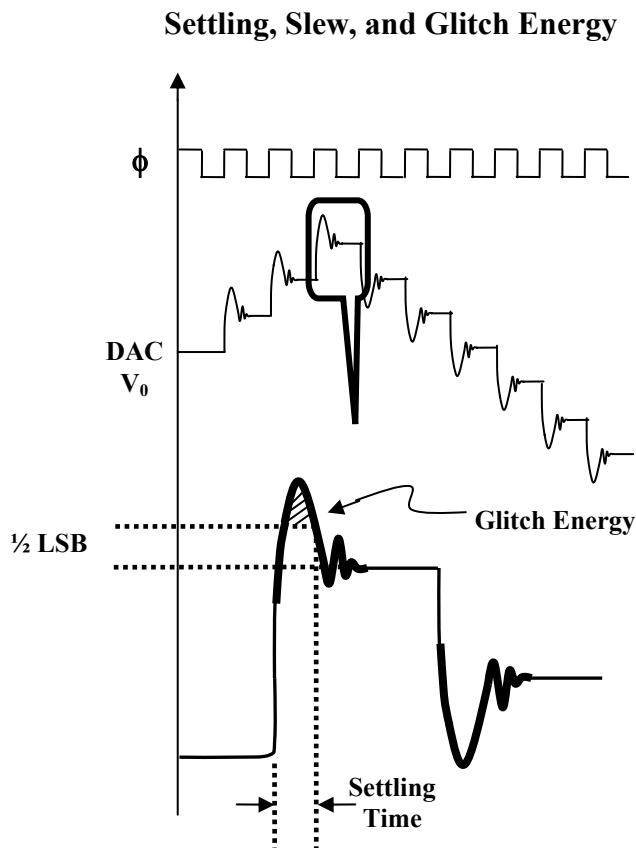


Figure 5.1

5.2 Crosstalk and Skew

Clock/data feed through is a broad term for any crosstalk from digital data lines or any clock to the DAC output. This is best observed by careful examination for high frequency modulation of the output during clock and data transactions (see Figure 5.2).

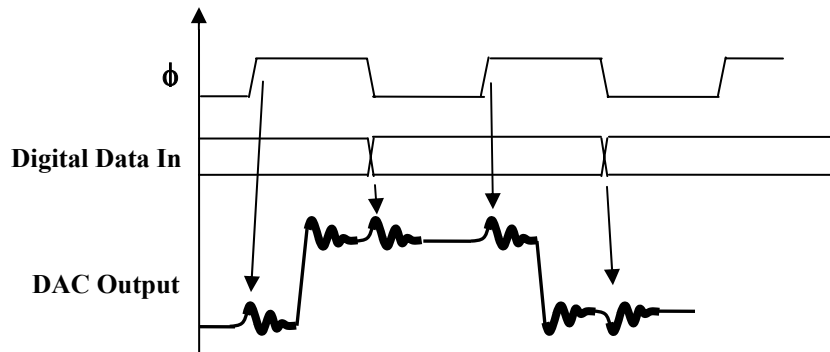


Figure 5.2

Another troublesome crosstalk is DAC output coupling back onto the sample clock. This can cause phase noise on the sample clock and degraded SFDR performance, often as increased spurs at even harmonics. It is best identified by careful examination of the sample clock for modulation that correlates with a monotone fundamental at the DAC output. Figure 5.3 shows cross modulation of the sample clock (trace 2) from the DAC differential outputs (traces 1 and 3). Figure 5.5 shows the resultant spectral spur from such crosstalk.

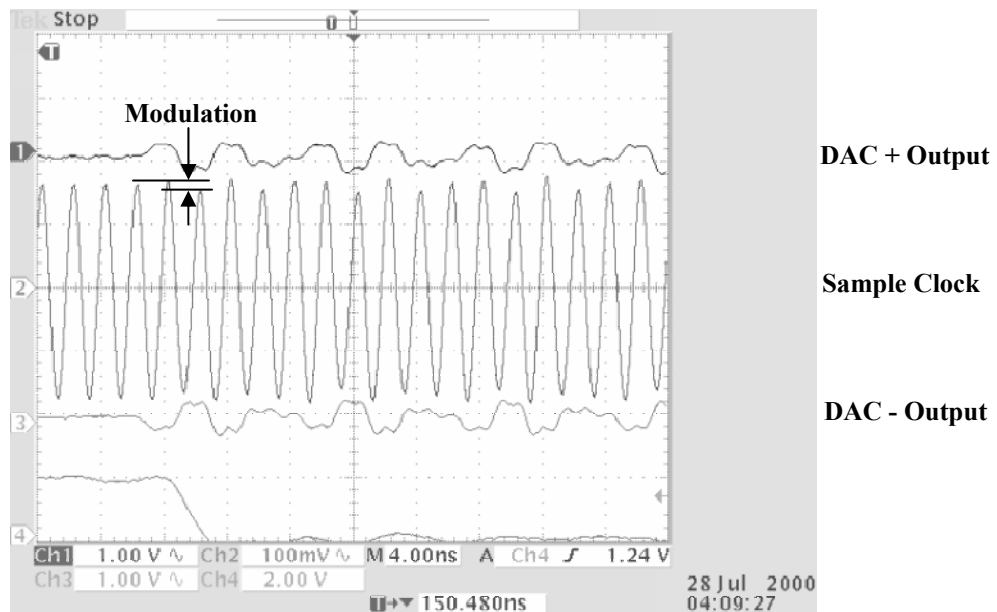


Figure 5.3

DAC to DAC skew is an important parameter for quadrature DAC pairs. It is also a difficult parameter to measure considering the large potential skew in instruments and transmission paths. If limits must be tested in production the best approach is to use focused calibration techniques to software deskew the sample clock and DAC output instrument and transmission paths for the DACs. Normally, skew is fixed by design and need only be observed with a high bandwidth scope. Be careful to place scope probes equidistant from the DUT.

5.3 Spectra

Reconstruction filters are significantly complex and costly. So telecom DACs are designed to minimize reconstruction complexity. The DAC output has significant high frequency energy in the step transition region that should not be ignored. The step energy is usually beyond the bandwidth of ATE digitizers. A high bandwidth continuous spectrum analyzer is usually needed for telecom DACs. The unfiltered staircase flat tops shift more energy to the low end of the spectrum based on the $\sin x/x$ rolloffⁱⁱ.

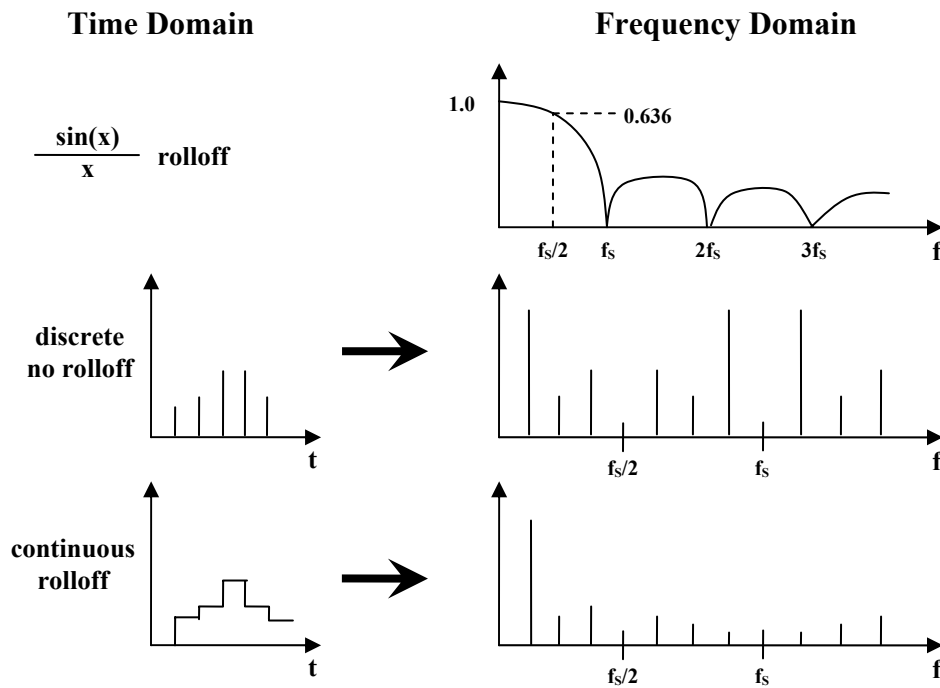


Figure 5.4

Discrete samples of near zero width produce discrete spectra that repeat in undiminished images at integer multiples F_s (mirrored at $F_s/2$). But when the samples fill the complete width $1/F_s$ the spectral power is attenuated by:

$$G(f) = \frac{\sin((\pi \times f) / F_s)}{((\pi \times f) / F_s)} \quad (\text{LSB}) \quad (5.1)$$

When taking continuous spectra from a staircased waveform one should correct the spectral magnitudes by an inverse factor of the $\sin x/x$ rolloff:

$$F_{\text{actor}}(f) = \frac{((\pi \times f) / F_s)}{\sin((\pi \times f) / F_s)} \quad (\text{LSB}) \quad (5.2)$$

Without this correction ratio measurements will be distorted. Harmonics above nyquist will be significantly attenuated. This correction is not needed when creating discrete spectra from discrete samples with DSP methods.

Signal to Noise Ratio (SNR) is the ratio of signal amplitude to noise amplitude expressed in dB. Noise content is computed as the orthogonal vector sum of the FFT noise bins (all excluding dc, fundamental and harmonics).

$$V_{\text{rms_noise}} = \sqrt{\sum_{i=1}^{N/2-1} V_{pki}^2} \quad (5.3)$$

$$\text{SNR} = V_{\text{rms_fund}} / V_{\text{rms_noise}} \quad (5.4)$$

Other signal to noise and distortion ratios are computed by the same method while excluding appropriate bin(s) magnitudes.

SFDR is an important parameter for high frequency telecom DACs. SFDR is a simple ratio of the fundamental to the largest spur. All the usual rules of DSP apply. An offending spur at an odd harmonic is likely related to amplitude distortion and at even harmonics is likely related to phase distortion.

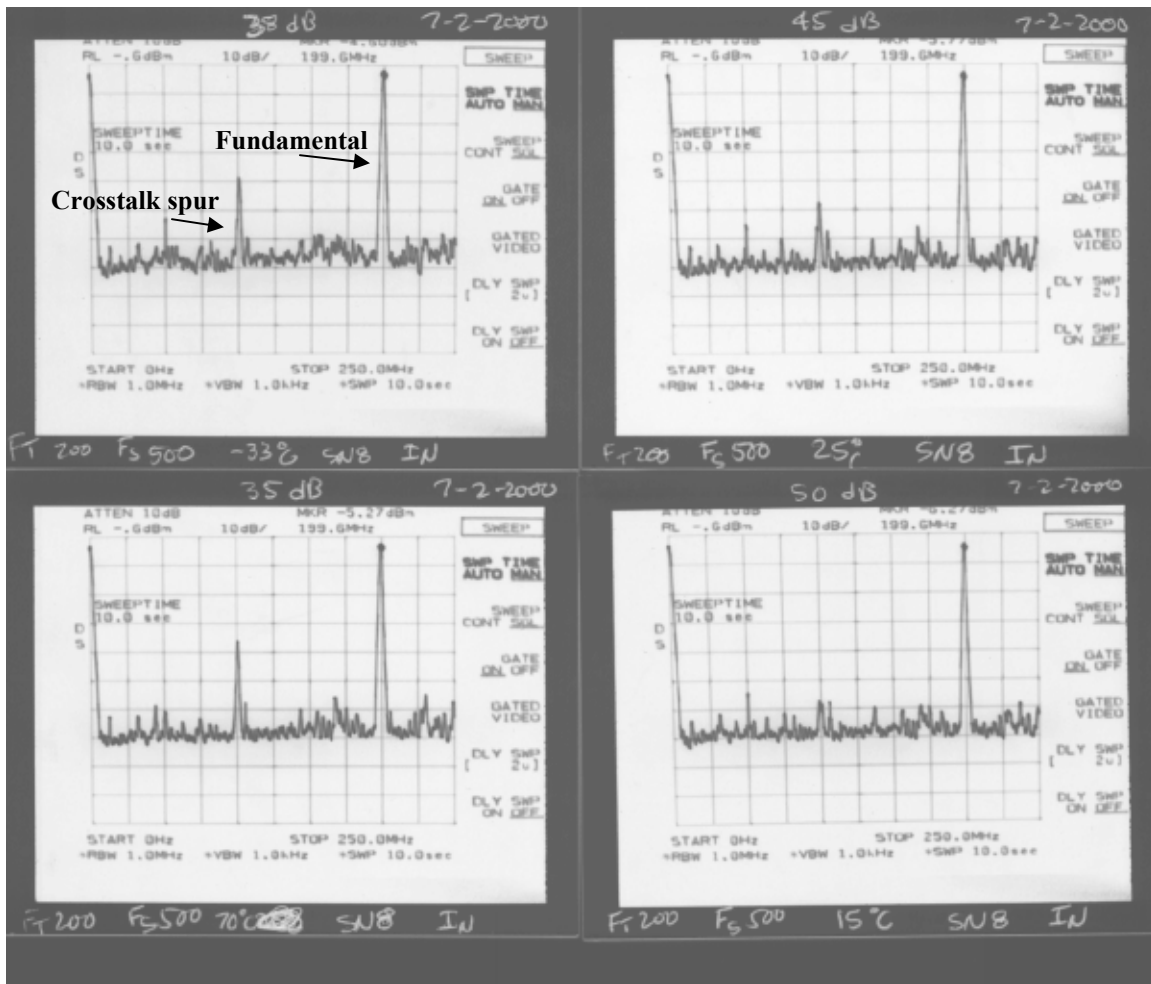


Figure 5.5

Figure 5.5 shows the continuous spectra of an unfiltered 8b DAC clocked at 500MHz with a 200MHz fundamental. The DAC was found to have output to sample clock crosstalk. This crosstalk essentially phase modulated the sample clock causing offending even harmonic spurs. Figure 5.5 shows the temperature sensitivity of the phenomena and identifies an SFDR sweet spot around 15°C.

Phase noise distortion can easily sneak into the ATE test set. As an example consider setting the clock frequency that is applied to the DAC. The ATE clock generator is phase synchronized by some high frequency super clock and smaller discretions are set based on some binary division of this primary super period. Since the DAC applied clock is an analog converted from a digital stored number it has the potential to exhibit phase quantization noise if it is not an integer multiple of the super period, just as any converter is subject to quantization noise around the LSB. One should either use only super period frequencies or carefully examine the clock for phase noise content (with spectrum analyzer).

Figure 5.6 shows a DAC with an output glitch. The problem is to determine what in the DAC architecture correlates with the glitch. What can you give the designer to help him determine the root cause?

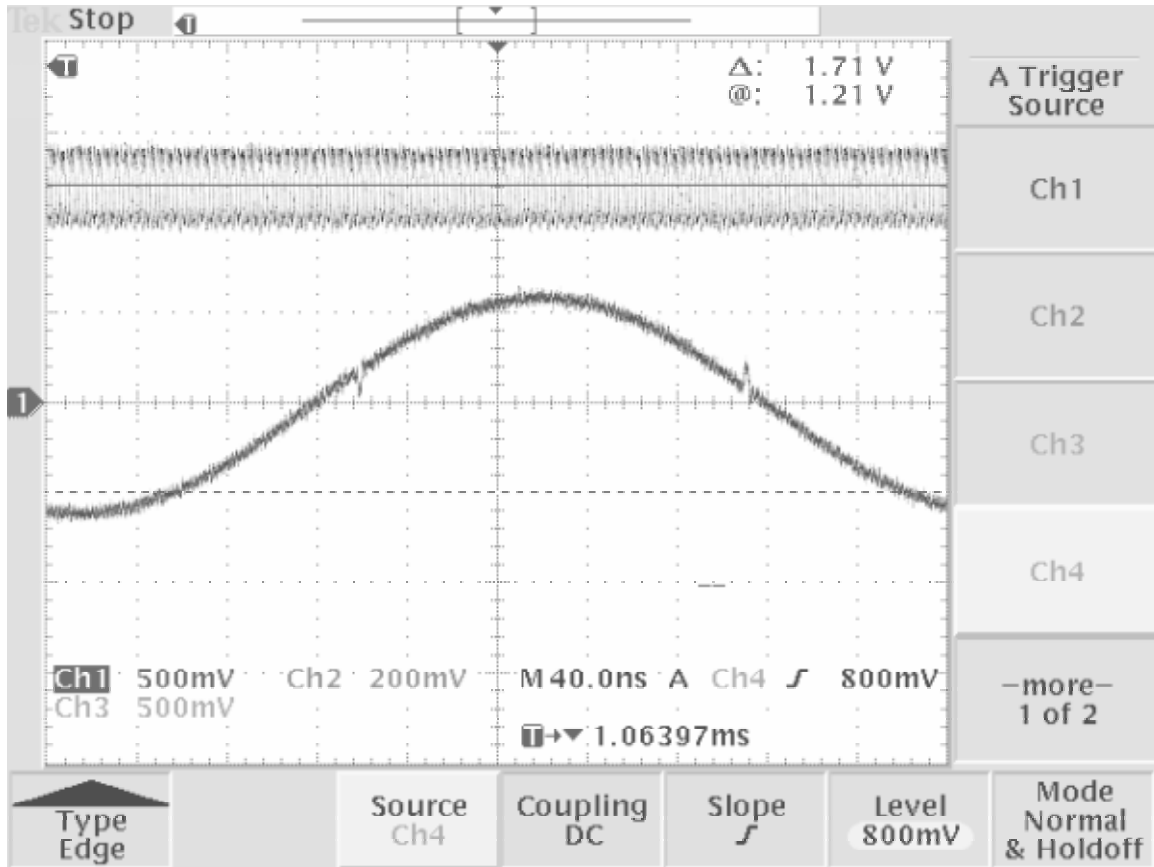


Figure 5.6

A useful pattern for exercising the DAC through stressful transitions is the bowtie pattern. The pattern consists of ping-ponging between complementary ramps. An example for a two's complement encoded 8b DAC is:

10000000 - 01111111 full scales
10000001 - 01111110
10000010 - 01111101
.
.
11111110 - 00000001
11111111 - 00000000 zero crossings
00000000 - 11111111
00000001 - 11111110
.
.
01111110 - 10000001
01111111 - 10000000 full scales
01111110 - 10000001
.
.
etc.

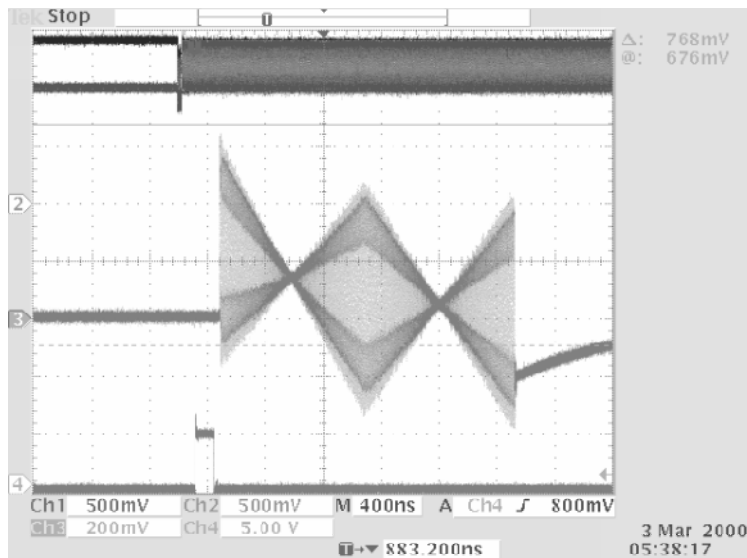


Figure 5.7

Figure 5.7 shows the time domain scope of the pattern. In this example the output shown is capacitively coupled and exhibits baseline settling for a short burst of the pattern. Close examination of the pattern can reveal anomalies at architectural boundaries known to the designer.

6 Load Board Guidelines

- 1) Use a single large mass ground plane common to both digital and analog signals. This makes maximum ground use of limited board real estate space and eliminates surprise dc and ac offsets.
- 2) Be very careful to separate the key signals (separate laminate planes or areas):
 - bandgap reference
 - digital data and clock (symbol)
 - analog clock (sample)
 - analog out
- 3) Carefully design transmission lines to avoid discontinuities. Terminate high frequency lines at both ends (when possible) allowing half amplitudes. Match differential and partner pair electrical lengths to the board design resolution limits. Place equidistant probe access on matched differential and partner pairs.
- 4) Liberally use high frequency coax and connectors on clocks and analogs to allow flexibility during debug.

ⁱ Mark Burns, Gordon W Roberts, *An Introduction to Mixed-Signal IC Test and Measurement*, Oxford University Press, 2001.

ⁱⁱ M. V. Mahoney, *Analog Test Concepts*, IEEE, 1987

For more information, please contact:

Craig Bousquet

President

TestEdge, Inc.

15930 Bernardo Center Drive

San Diego, CA 92127

Tel: (858) 451-1012 x308

E-mail: bousquet@testedgeinc.com

Bob Thomas

VP of Test Engineering

TestEdge, Inc.

15930 Bernardo Center Drive

San Diego, CA 92127

Tel: (858) 451-1012 x312

E-mail: rthomas@testedgeinc.com